PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMS/20/12148

Analog, MEMS & Sensors (AMS)

New assembly site (subcontractor TSHT China) for General Purpose Analog products in SOT23 package

WHAT:

Progressing on activities related to process modernization and quality improvement, ST is pleased to announce the introduction of TSHT/China as additional subcontractor for Assembly and Test & Finishing activities for some products assembled in our SOT23 package. Production is already running for general purpose analog products since 2017 on BCD6S and Bipolar technology.

Please find more information related to material change in the table here below

Material	Current process	Modified process	Comment
Diffusion location	St Crolles (France) / UMC (Taiwan)	St Crolles (France) / UMC (Taiwan)	No change
Assembly location	Carsem Malaysia	TSHT China	
Molding compound	Hitachi CEL 8240HF10	Hitachi CEL 1702HF9	
Die attach	Henkel QMI519	Henkel 8200T	
Leadframe	Copper	Copper	
Plating	NiPdAu	Matte Sn	
Wire	Gold 1mil	Copper Pd coated 1 mil	

WHY:
The purpose of the introduction of TSHT for both Assy and Test & Finishing activities for the here above listed commercial products is to further improve the rationalization of our manufacturing assets and provide a better support to our customers by enhancing the manufacturing process for higher volume production.

HOW:
The qualification program consists mainly of comparative electrical characterization and reliability tests.

You will find here after the qualification test plan which summarizes the various test methods and conditions that ST uses for this qualification program.

WHEN:
The new material set will be implemented in Q3/2020 in TSHT China.

Marking and traceability:

Unless otherwise stated by customer's specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales type, date code and lot number.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all the information reported on the relevant datasheets.

There is -as well- no change in the packing process or in the standard delivery quantities. Shipments may start earlier with the customer's written agreement.

Reliability Qualification plan

AMS Back-end qualification

Sot23-5

Production second sourcing to TSHT

General Information	
Product Line	*3021, UI69, KR33*
Product Description	Single high speed comparator, 200 mA low quiescent current very low noise LDO, Very Low Drop VREG @ 100mA 3.3 V
P/N	TS3021ILT, LDK120M-R, D2981ABM33TR
Product Group	AMS
Product division	General Purpose Analog &RF
Package	Sot23-5
Silicon Process technology	HF5CMOS, BCD6S, Bipolar (BI20II)

Locations	
Wafer fab	*UMC Taiwan , ST Catania (Italy), ST Singapore*
Assembly plant	*TSHT China*
Reliability Lab	*ST Grenoble, TSHT*

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify a new assembly site, TSHT China, for products in sot23-5Leads package for Analog products in HCMOS5/HF5CMOS technology based on existing qualification on BCD6S and Bipolar .

3.2 Conclusion

Qualification Plan requirements have to be fulfilled without issue. It is stressed that reliability tests have to show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests have to demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

❖ ***TS3021ILT***

life.augmented

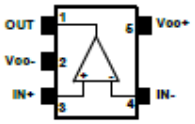
TS3021, TS3021A

Rail-to-rail 1.8 V high-speed comparator

Datasheet - production data

SOT23-5/SC70-5

Pin connections (top view)



Features

- Propagation delay: 38 ns
- Low current consumption: 73 µA
- Rail-to-rail inputs
- Push-pull outputs
- Supply operation from 1.8 to 5 V
- Wide temperature range: -40 °C to 125 °C
- High ESD tolerance: 5 kV HBM, 300 V MM
- Latch-up immunity: 200 mA
- SMD packages
- Automotive qualification

Related products

- TS3022 for a dual comparator with similar performances
- TS3011 for a high-speed comparator

Applications

- Telecom
- Instrumentation
- Signal conditioning
- High-speed sampling systems
- Portable communication systems

Description

The TS3021 single comparator features high-speed response time with rail-to-rail inputs. With a supply voltage specified from 2 to 5 V, this comparator can operate over a wide temperature range: -40 °C to 125 °C.

The TS3021 comparator offers micropower consumption as low as a few tens of microamperes thus providing an excellent ratio of power consumption current versus response time.

The TS3021 includes push-pull outputs and is available in small packages (SOT23-5 and SC70-5).

- The LDK120 low drop voltage regulator provides 200 mA of maximum current from an input supply voltage in the range of 1.9 V to 5.5 V, with a typical dropout voltage of 100 mV. It is stabilized with a ceramic capacitor on the output.
  The very low drop voltage, low quiescent current and low noise features make it suitable for low power battery-powered applications. An enable logic control function puts the LDK120 in shutdown mode allowing a total current consumption lower than 1 µA. The device also includes a short-circuit constant current limiting and thermal protection.

- The LD2981 is a 100 mA fixed-output voltage regulator. The low-drop voltage and the ultra low quiescent current make them suitable for low noise, low power applications and in battery powered systems.
  The quiescent current in sleep mode is less than 1 µA when INHIBIT pin is pulled low. Shutdown logic control function is available on pin n° 3 (TTL compatible). This means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. The LD2981 is designed to work with low ESR ceramic capacitor. Typical applications are in cellular phone, palmtop/laptop computer, personal digital assistant (PDA), personal stereo, camcorder and camera.

4.2 **Construction note**

	P/N TS3021ILT	***P/N LDK120M-R***	***P/N LD2981ABM33TR***
Wafer information			
Wafer fab manufacturing location	UMC Taiwan	ST Catania	ST Singapore
Technology	HF5CMOS	BCD6S	Bipolar
Die finishing back side	RAW SILICON	RAW SILICON	LappedSILICON
Die size (microns)	720x820 um	782 x 736 um	1470 x 990 um
Bond pad metallization layers	AlSiCu	AlCu	AlSi
Passivation type	PSG + NITRIDE	TEOS/SiN/Polyimide	P-Vapox/Nitride/Po-lyimide(PIQ)
Assembly information			
Assembly site	TSHT	TSHT	TSHT
Package description	Sot23-5leads	Sot23-5leads	Sot23-5leads
Molding compound	Hitachi CEL-1702HF9	Hitachi CEL-1702HF9	Hitachi CEL-1702HF9
Frame material	Cu	Cu	Cu
Die attach process	Epoxy Glue	Epoxy Glue	Epoxy Glue
Die attach material	Henkel 8200T	Henkel 8200T	Henkel 8200T
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Cu 1 mil Pd Coated	Cu 1 mil Pd Coated	Cu 1 mil Pd Coated
Lead finishing process	electroplating	electroplating	electroplating
Lead finishing/bump solder material	Matte Sn	Matte Sn	Matte Sn

5 TESTS PLAN SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	HF5CMOS/Sot23-5	3021	
2	BCD6S/Sot23-5	UI69	
3	Bipolar/Sot23-5	KR33	

5.2 Test plan summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					Note
						Lot 1 3021	Lot 2 UI69	Lot3 KR33			
HTB/ HTOL	N	JESD22 A-108	Ta = 125°C or 125°C, BIAS		168 H	77	0/77	0/77			
					1000 H	77	0/77	0/77			
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	50	0/50	0/50			
					500 H	50	0/50	0/50			
					1000 H	50	0/50	0/50			
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	Below sample + 22units	PASS	PASS			
UHAST	Y	JESD22 A-102	85%RH / Ta=130°C		96 H	77	0/75	0/75			
TC	Y	JESD22 A-104	Ta = -55°C to 150°C		100 cy	77	0/75	0/75			
					200 cy	77	0/75	0/75			
					500 cy	77	0/75	0/75			
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H	77	0/75	0/75			
					500 H	77	0/75	0/75			
					1000 H	77	0/75	0/75			

6 ANNEXES

6.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Description	Purpose
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.